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Attorney's Docket No.: 774-010234-US(PAR) *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: OOI et al. **Group No.:**
Serial No.: 09/802,084
Filed: 3/08/01 **Examiner:**
For: QUANTUM WELL INTERMIXING

Commissioner of Patents and Trademarks
Washington, D.C. 20231

TRANSMITTAL OF CERTIFIED COPY

Attached please find the certified copy of the foreign application from which priority is claimed for this case:

Country : **Singapore**
Application Number : **200004787-8**
Filing Date : **11 September 2000**

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NOTE: The claim to priority need be in no special form and may be made by the attorney or agent if the foreign application is referred to in the oath or declaration as required by § 1.63.

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REGISTRY OF PATENTS
SINGAPORE

This is to certify that the annexed is a true copy of the following Singapore patent application as filed in this Registry.

Date of Filing	:	11 SEPTEMBER 2000
Application Number	:	20004787-8
Applicant(s)	:	NANYANG TEHNOLOGICAL UNIVERSITY
Title of Invention	:	MULTIPLE WAVELENGTH LASERS

C. Chiang

CHIG KAM TACK
Assistant Registrar
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SINGAPORE

PATENTS FORM 1

Rule 19

SINGAPORE
THE PATENTS ACT
(CHAPTER 221)
THE PATENTS RULES

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1 1 SEP 2000

The Registrar of Patents,
Registry of Patents.

REQUEST FOR THE GRANT OF A PATENT

THE GRANT OF A PATENT IS REQUESTED BY THE UNDERSIGNED ON THE BASIS OF THE PRESENT APPLICATION.

I. Title of Invention		**MULTIPLE WAVELENGTH LASERS**
II. Applicant(s) (see note 2)	*(a) Name*	**NANYANG TECHNOLOGICAL UNIVERSITY**
	Body Description/ Residency	
	Street Name & Number	**SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING**
	City	**NANYANG AVENUE**
	State	
	Country	**SINGAPORE 639798**
	(b) Name	-
	Body Description/ Residency	
	Street Name & Number	
	City	
	State	
	Country	
	(c) Name	-
	Body Description/ Residency	
	Street Name & Number	
	City	
	State	
	Country	

200004787-8

III. Declaration of Priority (see note 3)	Country/ Country Designated		*File no.*	
	Filing Date			
	Country/ Country Designated		*File no.*	
	Filing Date			
	Country/ Country Designated		*File no.*	
	Filing Date			

IV. Inventors (see note 4)				
(a) The applicant(s) is/are the sole/joint inventor(s)	[ ]	*Yes*	[X]	*No*
(b) A statement on Patents Form 8 is/will be furnished.	[X]	*Yes*	[ ]	*No*

V. Name of Agent (if any) (see note 5)	**HAQ & NAMAZIE PARTNERSHIP**			
VI. Address for Service (see note 6)	*Block/Hse No.*		*Level No.*	
	~~Unit No~~/PO Box	**765**	*Postal Code*	**901515**
	Street Name	**Robinson Road Post Office**		
	Building Name			
VII. Claiming an earlier filing date under section 20(3),26(6) or 47(4). (see note 7)	*Application No.*			
	Filing Date			

[Please tick in the relevant space provided]:

(   ) Proceeding under rule 27(1)(a).

Date on which the earlier application was amended =__________

Or

(   ) Proceeding under rule 27(1)(b)

VIII. Invention has been displayed at an International Exhibition (see note 8)	☐ *Yes* ☒ *No*
IX. Section 114 requirement (see note 9)	*The invention relates to and/or used a micro-organism deposited for the purposes of disclosure in accordance with section 114 with a depositary authority under the Budapest Treaty.* ☐ *Yes* ☒ *No*
X. Check List (To be filled in by applicant or agent)	A. The application contains the following number of sheet(s):-

A. The application contains the following number of sheet(s):-		
1. Request	4	*sheets*
2. Description	15	*sheets*
3. Claim(s).	4	*sheets*
4. Drawing(s).	6	*sheets*
5. Abstract.	1	*sheets*

B. The application as filed is accompanied by:-	
1. Priority document	
2. Translation of priority document	
3. Statement of Inventorship & right to grant	X
4. International Exhibition Certificate	

XI. Signature(s) (see note 10)		
	Applicant (a)	
	Date	11 SEPT. 2000
	Applicant (b)	
	Date	
	Applicant (c)	
	Date	

NOTES :

1. This form when completed, should be brought or sent to the Registry of Patents together with the prescribed fee and 3 copies of the description of the invention, and of any drawings.

2. Enter the name and address of each applicant in the spaces provided at paragraph II. Names of individuals should be indicated in full and the surname or family name should be underlined. The names of all partners in a firm must be given in full. The place of residence of each individual should also be furnished in the space provided. Bodies corporate should be designated by their corporate name and country of incorporation and, where appropriate, the state of incorporation within that should be entered where provided. Where more than three applicants are to be named, the names and address of the fourth and any further applicants should be given on a separate sheet attached to this Form together with the signature of each of these further applicants.

3. The declaration of priority at paragraph III should state the date of the previous filing, the country in which it was made, and indicate the file number, if available. Where the application relied upon in an International Application or a regional patent application e.g. European patent application, one of the countries designated in that application [being one falling under the Patents (Convention Countries) Order] should be identified and the name of that country should be entered in the space provided.

4. Where the applicant or applicants is/are the sole inventor or the joint inventors, paragraph IV should be completed by marking the 'YES' Box in the declaration (a) and the 'NO' Box in the alternative statement (b). Where this is not the case, the 'NO' Box in declaration (a) should be marked and a statement will be required to be filed on Patents Form 8.

5. If the applicant has appointed an agent to act on his behalf, the agent's name should be indicated in the spaces available at paragraph V.

6. An address for service in Singapore to which all documents may be sent must be stated at paragraph VI. It is recommended that a telephone number be provided if an agent is not appointed.

7. When an application is made be virtue of section 20(3), 26(6) or 47(4), the appropriate section should be identified at paragraph VII and the number of the earlier application or any patent granted thereon identified.

8. Where the applicant wishes an earlier disclosure of the invention by him at an International Exhibition to be disregarded in accordance with section 14(4)©, then the 'YES' box at paragraph VIII should be marked. Otherwise the 'NO' box should be marked.

9. Where in disclosing the invention the application refers to one or more micro-organisms deposited with a depository authority under the Budapest Treaty, then the 'YES' box at paragraph IX should be marked. Otherwise the 'NO' box should be marked.

10. Attention is drawn to rules 90 and 105 of the Patent Rules. Where there are more than three applicants, see also Note 2 above.

11. Applicants resident in Singapore are reminded that if the Registry of Patents considers that an application contains information the publication of which might be prejudicial to the defence of Singapore or the safety of the public, it may prohibit or restrict its publication or communication. Any person resident in Singapore and wishing to apply for patent protection in other countries must first obtain permission from the Singapore Registry of Patents unless they have already applied for a patent for the same invention in Singapore. In the latter case, no application should be made overseas until at least two months after the application has been filed in Singapore.

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MH/JN/jp/5000811SGF

20000 4787-8
11 SEP 2000

MULTIPLE WAVELENGTH LASERS

Field of the Invention

The present invention relates to laser structures for providing plural different radiation wavelengths and to a method of manufacturing such lasers.

Background of the Invention

The growth of Internet traffic, multimedia services and high-speed data services has exerted pressure on telecommunication carriers to expand the capacity of their networks quickly and cost effectively. The three options normally available are:

1) Install new fibers,

This has problems due to costs and difficulties of rights of way.

2) Increase the bit rate of the transmission system.

This option has inherently limited growth potential.

3) Employ wavelength division multiplexing.

This third option allows manifold increase of the network capacity at a modest cost.

Wavelength division multiplexing, also known as frequency division multiplexing, allows better use of the available bandwidth by carrying plural optical transmission channels over a single fiber. Each channel operates at a different frequency/wavelength. Alternatively data may be sent in packets each at different frequencies or wavelengths.

Wavelength division multiplex transmission systems may also enable longer span distance between repeaters, and more spans before regeneration is needed. This makes such systems attractive for long haul transmission.

The heart of the wavelength division multiplexing systems is a multiple-wavelength laser device. In known commercial devices using distributed feedback lasers, the laser wavelength may be tuned by defining gratings with a submicron period to perform frequency chirp. The device grating is conventionally formed by electron beam lithography, as holography has not been found suitable for creation of complex multi-pitch grating structures. Electron beam writers are however costly and of low throughput. Thus electron beam lithography is not favourable for large-scale device production. In addition, regrowth of the sample is necessary, and this entails additional cost.

Alternatively selective area epitaxial growth has been used to fabricate multiple wavelength lasers. This technique utilizes differences in epitaxial layer composition and thickness produced by growth through a mask to achieve spatially selective bandgap variation. This process works well under a precisely controlled set of parameters but is difficult to manipulate in a generic fashion.

Each of the methods of the prior art has disadvantages. For example, using etching and regrowth methods results in poor optical confinement to the wave-guide devices as a result of sidewall inhomogeneity. As it involves

multiple processing steps there is often a low yield and throughput may be low.

Selective area epitaxy is also a complicated technique and requires complex steps of sample preparation. Also, the technique may give non-uniform growth rate across the strip that prevents subsequent planar processing. For the same reason, passive wave-guide sections may be relatively lossy.

Quantum well intermixing can be used selectively to modify the bandgap energy of a quantum well sample. However, spatial control of the bandgap using the prior art quantum well intermixing techniques is complicated. For example using varying thickness of silicon dioxide layers as intermixing sources of impurity-free vacancy disordering, or implant masks for impurity induced disordering (IID) increases the number of processing steps of lithography and deposition of dielectric caps.

To overcome this complexity the prior art includes a one-step spatially controlled quantum well intermixing technique based upon impurity-free vacancy disordering. In this process, the semiconductor is patterned with very small areas of SrF_2 followed by coating the sample with SiO_2. The degree of intermixing then depends on the area of semiconductor substrate in direct contact with the SiO_2 layer. This technique, although being one-step, requires electron beam lithography, which decreases the process throughput and increases design complexity.

It is accordingly an object of the present invention to at least partially mitigate the difficulties of the prior art.

Summary of the Invention

According to one aspect of the invention there is provided a laser structure, said structure comprising a plurality of quantum well regions on a semiconductor substrate, each said region containing a respective different concentration of an impurity, to thereby provide a corresponding plurality of different radiation wavelengths in use.

Embodiments of the invention include monolithically integrated multiple-wavelength laser structures in 1.55 μm GaInAs/GaInAsP materials. Typical embodiments have more than 5 channels and are produced using a low energy IID process.

According to a further aspect of the present invention there is provided a method of manufacturing a photonic integrated circuit comprising providing a structure having a quantum well region, and performing quantum well intermixing, characterized in that said step of performing quantum well intermixing comprises differentially masking portions of said region, implanting impurities into said differentially masked portions and annealing said structure.

Preferably said step of differentially masking portions of said region comprises forming a masking layer on said

portion of said region and differentially etching said masking layer.

Advantageously before said etching step the method comprises forming a photoresist on said masking layer, applying masks having different optical densities to said photoresist and developing said photoresist.

Conveniently said step of forming a photoresist may comprise spin-coating said photoresist on said masking layer.

Conveniently said masking layer comprises a dielectric such as silicon dioxide. Alternatively said masking layer may comprise a polymer or a metal.

Preferably said etching step comprises dry etching.

Advantageously said dry etching has substantially a one-to-one selectivity between photoresist and said masking layer.

Conveniently process parameters of the said dry etching system are selected to provide said selectivity.

Conveniently said annealing step is performed in a rapid thermal processor, alternatively a rapid thermal annealer or furnace may be used.

Preferably said impurities comprise phosphorus and arsenic.

Brief Description of the Drawings

An exemplary embodiment of the invention will now be described with reference to the accompanying drawings in which: -

Figure 1 shows in diagrammatic form a typical quantum well structure used in the present invention;

Figure 2 shows an exemplary process flow for fabrication of multiple wavelength lasers;

Figure 3(a) and (b) show the thickness of resist and oxide before and after reactive ion etching;

Figure 4(a) to (c) show the results of measurements on the first embodiment of the invention and;

Figure 5(a) to (c) shows the results of measurements on the second embodiment.

Description of the Preferred Embodiments

In the various figures, like reference numerals refer to like parts.

Referring to Figure 1, an exemplary semiconductor structure suitable as the basis for manufacturing multiple wavelength lasers was formed. An InP/Ga_{1-x}

$In_xAs/Ga_{1-x}In_xAs_yP_{1-y}$ structure (10) was grown using metal organic chemical vapour deposition (MOCVD) on an InP substrate. An active region was formed, comprising a single undoped quantum well region consisting of a 5.5 nm wide GaInAs quantum well (14), and 12 nm GaInAsP (λ_g=1.26μm) barriers (22,24). The active region was bounded by step or graded index (GRIN) GaInAsP confining layers (20-21, 25-26). The confining layers comprise 50nm of material having λ_g=1.18 μm and 80nm of material having λ_g=1.05 μm, respectively. The structure was lattice matched to InP throughout, and was completed with a 1.4 μm InP upper cladding layer (28) and a layer (30) of 0.65 μm GaInAsP followed by a 0.1μm GaInAs layer (32) forming a contact layer. The lower cladding layer (12) was Sulphur-doped to a concentration of 2.5×10^{18} cm^{-3}. The upper cladding layer (28) was doped with Zn to a concentration of 7.4×10^{17} cm^{-3} and the subsequent layers (30,32) were doped with 2×10^{18} cm^{-3} and 1.3×10^{19} cm^{-3} concentration of Zn respectively. The core of the structure, forming a wave-guide, was undoped, thus forming a P-I-N structure with its intrinsic region restricted to the quantum well and GRIN layers.

Referring now to Figure 2, an outline of the process of the invention will now be given: -

Two embodiments of the invention are provided. In the first, a quantum well structure (such as that described with respect to Figure 1) was implanted with As impurities that varied in amount spatially by virtue of implantation through a varying thickness gray mask. In

the second, a similar type of mask was used to implant P ions in a similar way.

Simulations of the impurity implantation ranges and vacancy distribution were first carried out to determine the thickness of SiO_2 required for the bandgap shift that was sought. It would alternatively be possible to use other theoretical calculations or empirical approaches.

The thickness of SiO_2 mask required to totally block As ions from reaching the semiconductor during implantation was found to be around 400 nm. The thickness of SiO_2 mask required to totally block P ions from reaching the semiconductor during implantation was found to be around 900 nm.

In step (i) laser isolation and alignment mark etching is performed, for example using a first mask having a 20μm stripe pattern. An exemplary etching process is a wet-etching process using sulphuric acid, hydrogen peroxide and water in 1:8:40 ratio whereby 0.15μm of the GaInAs and GaInAsP contact layer is removed.

After the laser isolation and alignment mark etching step the structure is coated with oxide to the above respective thickness according to the impurity to be used, to act as a mask.

It will be understood that masks other than oxide could be used, for example, polymer, metal or photoresist mask materials, or dielectrics other than oxide.

Next, a positive photoresist is spin-coated onto the structure.

In step (ii), photolithography is carried out to transfer the gray patterns onto the structure: -

The gray mask technique of the invention makes use of different transparencies of masks to control the degree of the exposure of photoresist at selected regions and thus different thickness of photoresist after development. The degree of the development of photoresist after UV exposure has a linear relationship with the optical density. In the current embodiments, gray mask was selected having 10 levels, from 0.15 to 1.05 with a step of 0.1, of optical density, see Figure 4. By this means, it was intended to provide 10 different bandgaps after quantum well intermixing. It will of course be clear to those skilled in the art that fewer or greater numbers of bandgaps could be provided, according to the requirements of the application.

The relationship between optical density of mask and the UV light transmissivity level during the lithography process can be expressed using the following equation.

$$OD = -\log (T)$$

where OD is optical density and T is transmissivity.

In step (iii), a dry etching process is performed so as to etch correspondingly into the oxide mask, so that different thicknesses of oxide are produced in correspondence with the gray masking.

For the embodiments, a reactive ion etching process with 1:1 selectivity between photoresist and SiO_2 was chosen as the dry etching process. This process was performed in a conventional parallel plate radio-frequency reactive ion etching system using CF_4 and O_2 as process gases. Statistical methods were then used to optimise the parameters of this novel non-selective reactive ion etching process. To achieve 1:1 non-selective etching, the following settings were found suitable for the particular materials in question: pressure of 95~120 mTorr, RF power 40~100 W, CF_4 flow rate 20~80 standard cubic centimetre per minute (sccm) and O_2 flow rate 1~10 sccm.

The thickness of the resist and SiO_2, as measured from a surface profiler, both before and after reactive-ion etching for the two embodiments are given in Figure 3a and 3b. The first embodiment (As^{++} implanted -Fig. 3a) shows a slightly inferior quality of gray level transition; also saturation of pattern thickness at both the upper and the lower density regions are detected. This effect is mainly due to the thin resist required for the As^{++} implanted sample, which causes imperfect gradation after development. With the imperfect gradation, the SiO_2 pattern profile is directly affected.

However, for the second embodiment (P^{++} implanted-Fig. 3b) smooth and obvious transitions at each density levels are obtained.

In step (iv), implantation is carried out with impurity ions through the mask. In the embodiments, the samples

were implanted with $1x10^{14}$ cm^{-2} at 350~500 keV for both As and P impurities, at 150~230 °C. The result of the implantation through the masks is that the degree of implantation is inversely proportional to the thickness of the graded masks.

In step (v), quantum well intermixing step was carried out by annealing using a rapid thermal processor, at 500~800 °C for about 80~120 s along with the SiO_2 implant mask intact. The SiO_2 implant mask was removed after quantum well intermixing.

After this, laser fabrication was completed as follows: -

a) front contacts (p-type: Ti/Au, 50 nm/200 nm) were metallised using an electron beam evaporator.

b) the samples were then thinned to a thickness of around 180µm.

c) a metallisation for the back contact (n-type: Au/Ge/Au/Ni/Au, 14nm /14nm /14nm /11nm /200nm) was performed by evaporation;

d) a metal lift-off step for the laser isolation trench was performed. The heavily doped GaInAs and GaInAsP contact layers were removed at the trenches to achieve good electrical isolation between lasers.

e) the whole fabrication was completed by annealing the samples using rapid thermal processing at 300~450 °C for 45~100 s.

The lasers were then cleaved for testing. Each individual laser has a dimension of 400 x 500µm² and 50µm width of active window, 500µm cavity length and 20µm width of isolation trench.

In step (vi), the testing step, intensity vs. current and spectrum measurements were carried out. Each laser was pumped individually during the characterisation and measurements.

A linear correlation between thickness of implant mask and the wavelength emission was found in Figures 4a and 5a. This further verifies the linear relationship between the degree of point defects generated with different thickness of implant mask and the degree of intermixing or bandgap-tuning.

As shown in Fig 4b, in the first embodiment, using As impurities, a 6-channel monolithic multiple wavelength laser structure was achieved. The wavelengths were 1.555 μm, 1.544 μm, 1.535 μm, 1.518 μm, 1.503 μm, and 1.484 μm respectively.

As shown in Fig 5b, in the second embodiment, using P impurities, a 10 channel monolithic multiple wavelength laser structure was achieved. The wavelengths were 1.557 μm, 1.555 μm, 1.550 μm, 1.548 μm, 1.543 μm, 1.530 μm, 1.514 μm, 1.487 μm, 1.479 μm and 1.474 μm respectively.

The reason for not achieving 10-channels in the first embodiment is because the gray levels were found to saturate outside the gray 3 to gray 8 region. This explains the reason why certain channels give similar lasing wavelength after quantum well intermixing.

After measuring the light-current characteristics of the As^{++} and P^{++} multiple wavelength lasers, the threshold currents and the slope efficiencies were then analysed (Fig. 4c and 5c).

For the first embodiment, As^{++}-IID lasers fabricated from regions with SiO_2 completely removed suffered from a 25 % increase in threshold current, from 1.6 kA/cm^2 to 2 kA/cm^2 (Figure 4c).

For the second embodiment, only a 17 % increase of threshold current density, from 1.2 kA/cm^2 to 1.4 kA/cm^2 was observed between the non-implanted (gray 1: full oxide, non-intermixed but annealed) and direct implanted (gray 10: no oxide, fully intermixed and annealed) regions -- see Figure 5c.

However, for both embodiments, the slope efficiency shows very little change. This indicates that the quality of the materials remains high after intermixing using the technique of the invention.

The method of the invention may be used to produce other components as well as multi-frequency devices because the material produced is of high electrical and optical quality. Thus the technique is suited to the production of photonic integrated circuits.

Although the present invention has been described using a specific compound semiconductor, it is applicable to other compound semiconductors. The embodiment has been described using oxide as the mask but it will be

understood by those skilled in the art that any suitable dielectric can be used or indeed that a polymer or metal mask can be used instead. In the described embodiment a mask was used as well as a photoresist but it will also be clear to those skilled in the art that a graded photoresist could be used without an additional mask. The embodiment has been described in the context of a rapid thermal processor but rapid thermal annealers, furnaces and other temperature devices may be used instead.

It is also understood by those skilled in the art that routine practices including the following can be applied to enhance the performance and functionality of the said multi-wavelength laser diodes:-

1) Optical gratings can be incorporated in the laser structure to provide distributed feedback to the laser arrays, and also to provide fine-tuning of the lasing wavelengths to specified values. Such distributed feedback lasers or distributed Bragg reflecting lasers allows for an improved narrow spectral line-width and good side-mode suppression.
2) The optical outputs from the multi-wavelength laser arrays can be combined together in an integrated passive coupler or monolithic multimode-interference combiner for transmission into an optical modulator, optical amplifier, or launching into an optical fiber.
3) Optical coatings of specified reflectivity could be applied to the facets of the device to enhance its output efficiency.

Although the described embodiments relate to laser diode arrays emitting around 1.5 μm, the process technology can also be used to form devices operating at other wavelengths. It is understood therefore that the structures of the invention are not restricted to any specific wavelength.

CLAIMS:

1. A laser structure comprising a plurality of quantum well regions on a semiconductor substrate, wherein each said region contains a respective different concentration of an impurity, to thereby provide a corresponding plurality of different radiation wavelengths in use.

2. The laser structure of claim 1 wherein said substrate is a III-V semiconductor material.

3. The laser structure of claim 2 wherein said material comprises InGaAs.

4. The laser structure of any preceding claim wherein said impurity comprises As.

5 The laser structure of any of claims 1-3 wherein said impurity comprises P.

6. The laser structure of any preceding claim wherein each said region comprises a quantum well intermixed region.

7. An integrated circuit comprising the structure of any preceding claim, and electrical connections for applying respective pumping signals to said regions.

8. A method of manufacturing a laser structure capable of emitting different radiation wavelengths comprising providing a semiconductor substrate, forming a quantum well region therein, characterised by: differentially masking portions of said region, implanting impurities into said differentially masked portions, and annealing said structure whereby each said portion in use emits a respective one of said different radiation wavelengths.

9. The method of claim 8 wherein said step of differentially masking portions of said region comprises forming a masking layer on said portion of said region and differentially etching said masking layer.

10. The method of claim 9 wherein before said etching step, the method comprises forming a photoresist on said masking layer, applying masks having different optical densities to said photoresist and developing said photoresist.

11. The method of claim 10 wherein said step of forming a photoresist comprises spin-coating said photoresist on said masking layer.

12. The method of any of claims 9-11 wherein said masking layer comprises a dielectric.

13. The method of claim 12 wherein said dielectric is silicon dioxide.

14. The method of any of claims 9-11 wherein said masking layer comprises a polymer.

15. The method of any of claims 9-11 wherein said masking layer comprises a metal.

16. The method of claim 9 wherein said etching step comprises dry etching.

17. The method of claim 16 wherein said dry etching has a one-to-one selectivity between photoresist and said masking layer.

18. The method of claim 17 wherein process parameters of a dry etching system are selected to provide said one-to-one selectivity.

19. The method of claim 8 or claim 9 wherein said step of differentially masking portions of said region comprises using a graded photoresist.

20. The method of any of claims 8-19 wherein said step of implanting impurities comprises ion implantation.

21. The method of any of claims 8-19 wherein said step of implanting impurities comprises a focused ion beam technique.

22. The method of any of claims 8-19 wherein said step of implanting impurities comprises diffusion.

23. The method of any of claims 8-22 wherein said annealing step is performed in a rapid thermal processor.

24. The method of any of claims 8-23 wherein said annealing step uses a rapid thermal annealer.

25. The method of any of claims 8-22 wherein said annealing step is performed in a furnace.

26. The method of any of claims 8-25 wherein said impurities comprise phosphorus.

27. The method of any of claims 8-25 wherein said impurities comprise arsenic.

ABSTRACT

MULTIPLE WAVELENGTH LASERS

A multiple wavelength laser has plural quantum well regions on a substrate, each region containing a respective different concentration of an impurity to provide plural radiation wavelengths.

An impurity induced disordering technique using a gray mask is also described.

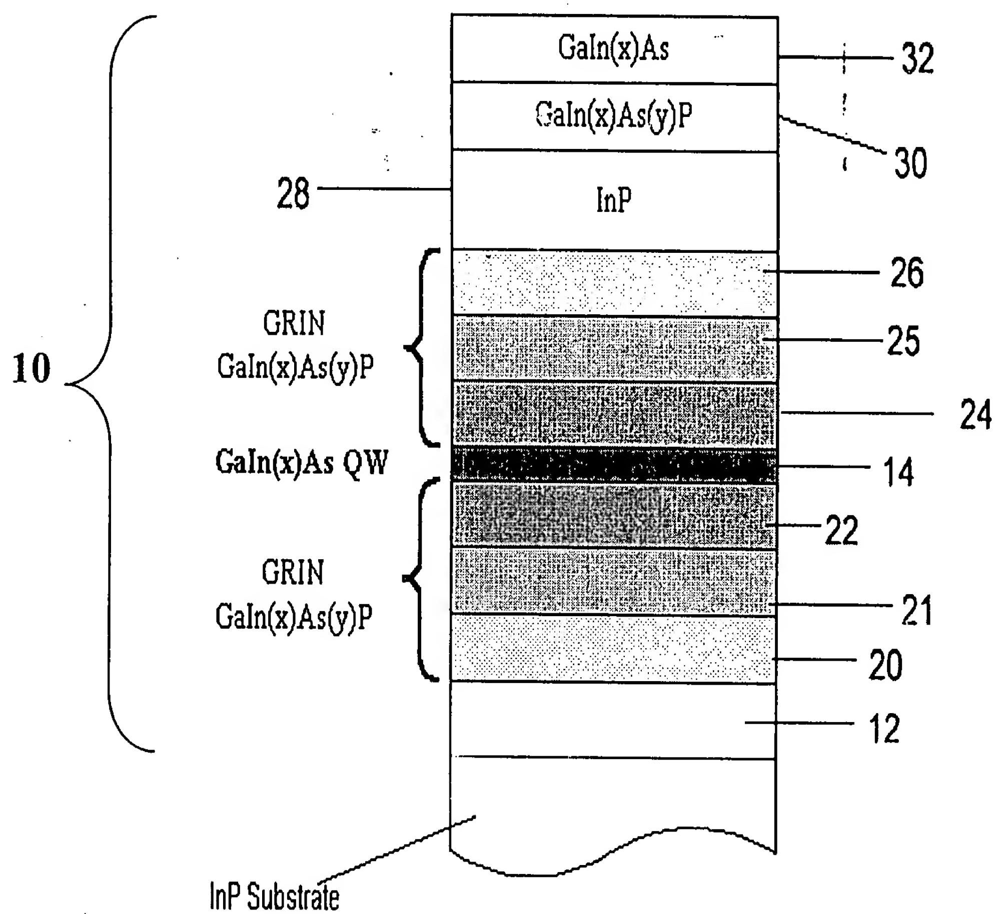
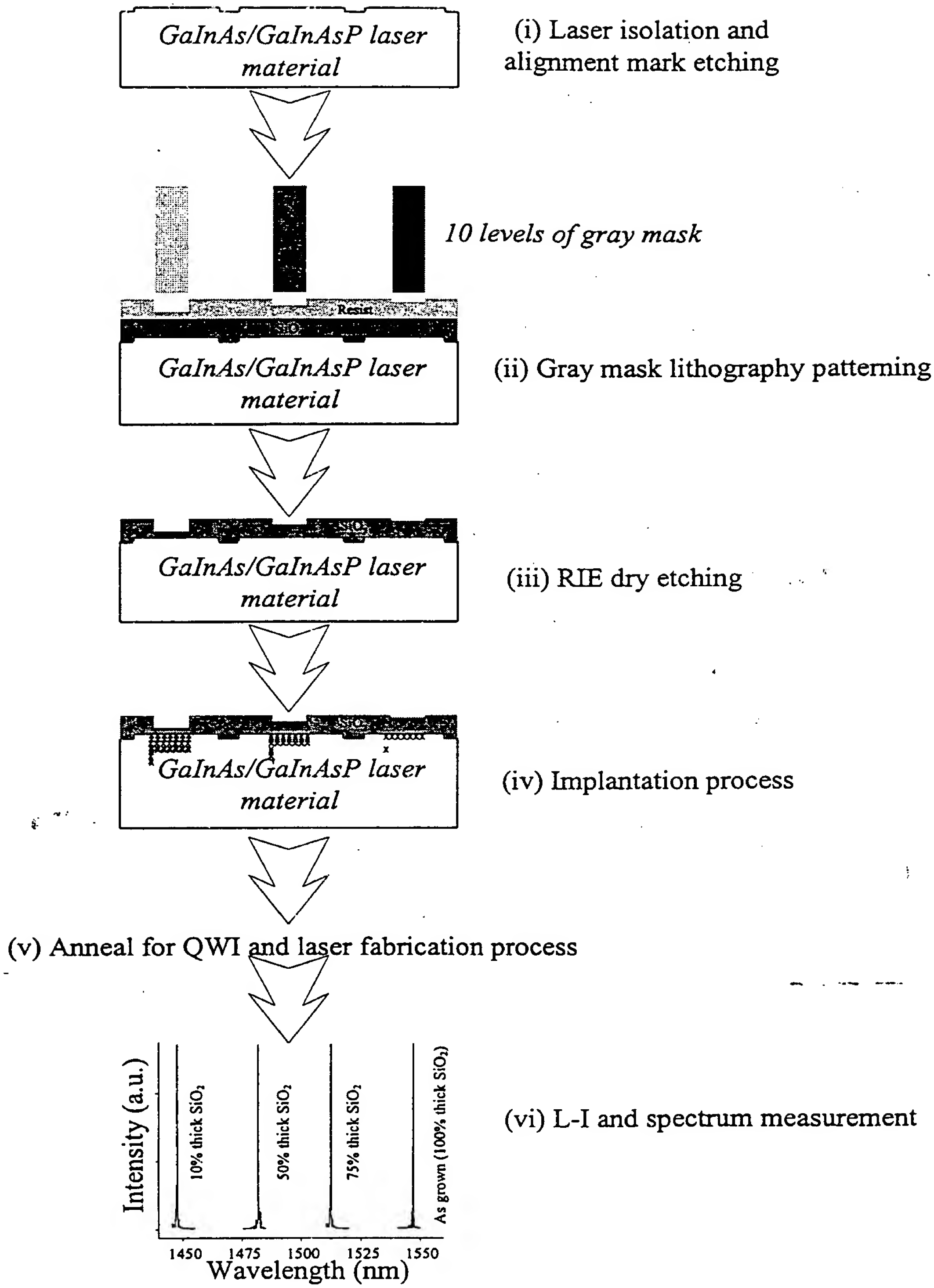
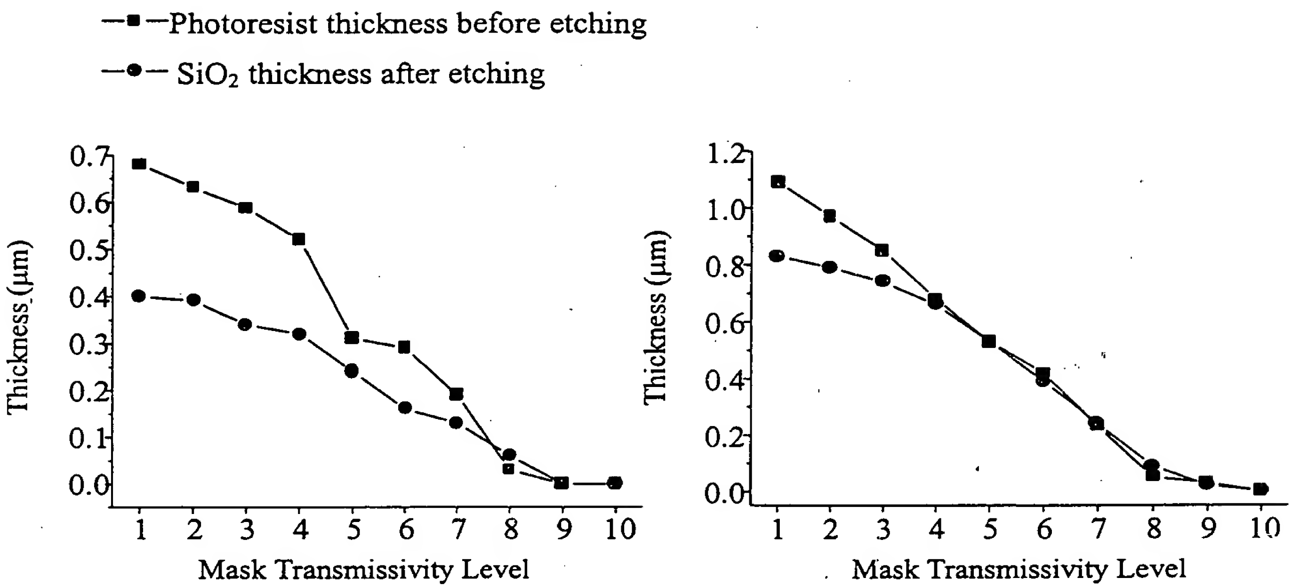

GaIn(x)As
GaIn(x)As(y)P
InP
GRIN
GaIn(x)As(y)P
GaIn(x)As QW
GRIN
GaIn(x)As(y)P
InP Substrate
10
28
32
30
26
25
24
14
22
21
20
12

Figure 1



GaInAs/GaInAsP laser material
(i) Laser isolation and alignment mark etching
10 levels of gray mask
Resist
SiO
GaInAs/GaInAsP laser material
(ii) Gray mask lithography patterning
GaInAs/GaInAsP laser material
(iii) RIE dry etching
GaInAs/GaInAsP laser material
(iv) Implantation process
(v) Anneal for QWI and laser fabrication process
Intensity (a.u.)
10% thick SiO_2
50% thick SiO_2
75% thick SiO_2
As grown (100% thick SiO_2)
1450
1475
1500
1525
1550
Wavelength (nm)
(vi) L-I and spectrum measurement

Figure 2



—■—Photoresist thickness before etching
—●— SiO2 thickness after etching
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
Thickness (μm)
1 2 3 4 5 6 7 8 9 10
Mask Transmissivity Level
1.2
1.0
0.8
0.6
0.4
0.2
0.0
Thickness (μm)
1 2 3 4 5 6 7 8 9 10
Mask Transmissivity Level

(a) (b)

Figure 3

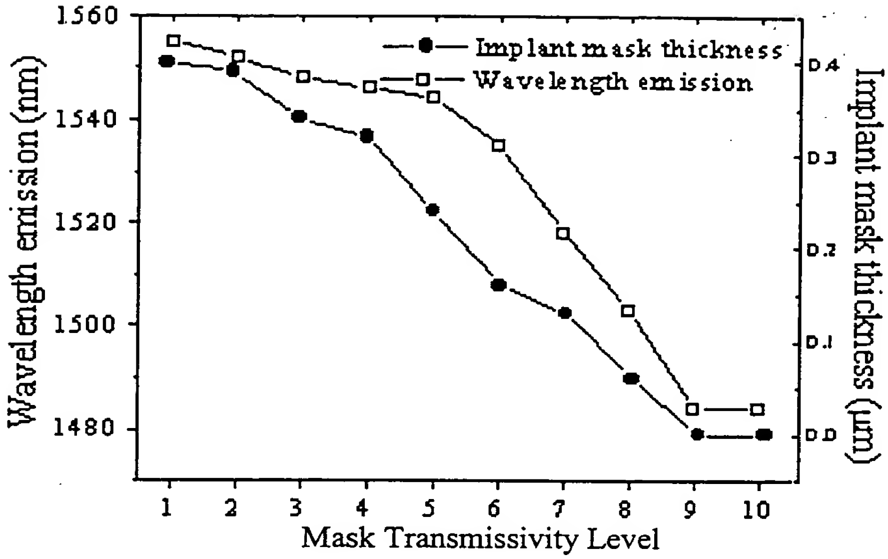


Figure 4(a)

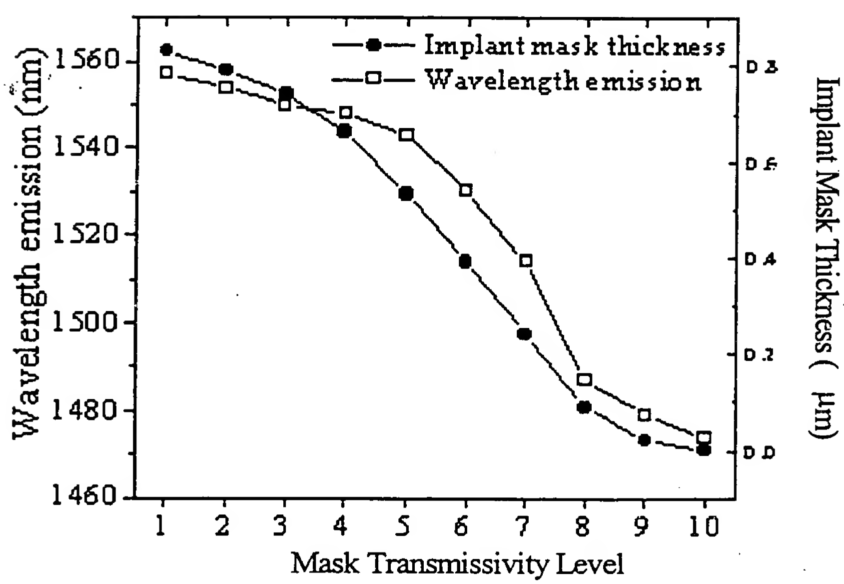


Figure 5(a)

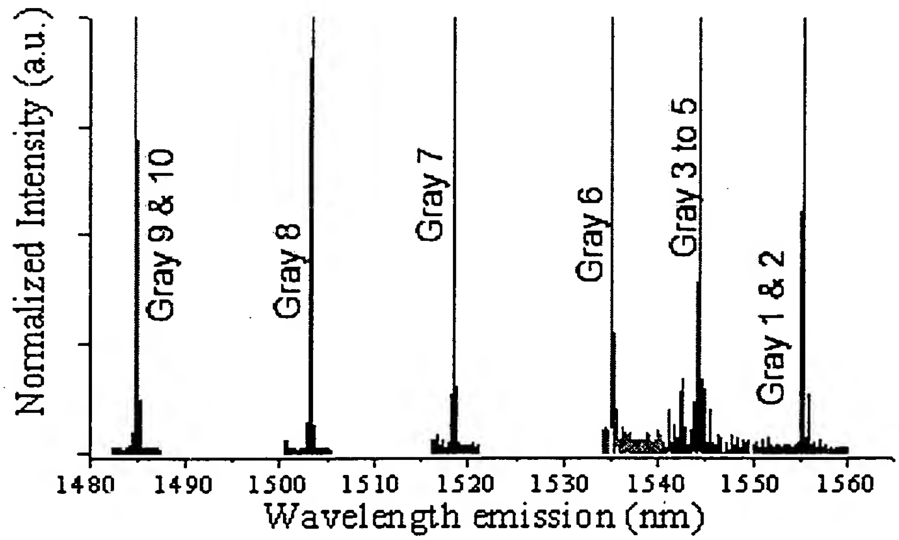


Figure 4(b)

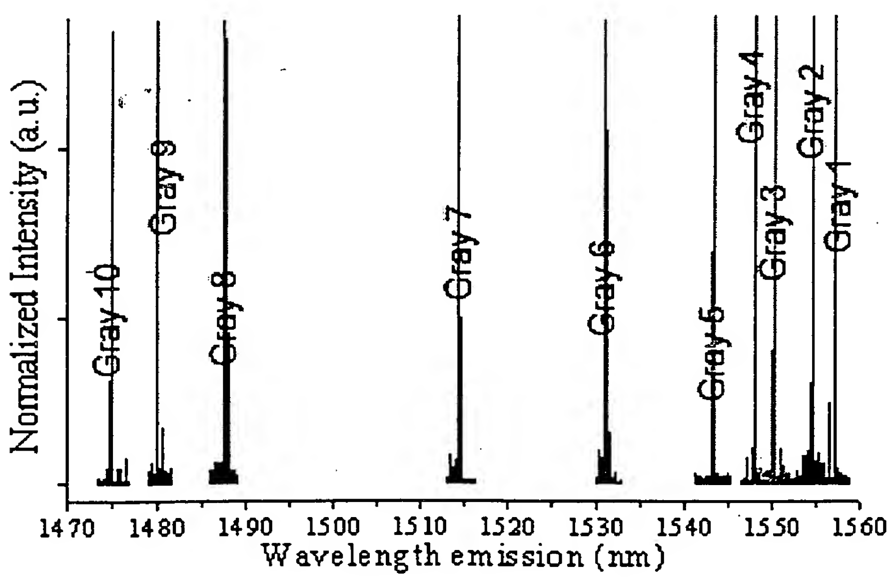


Figure 5(b)

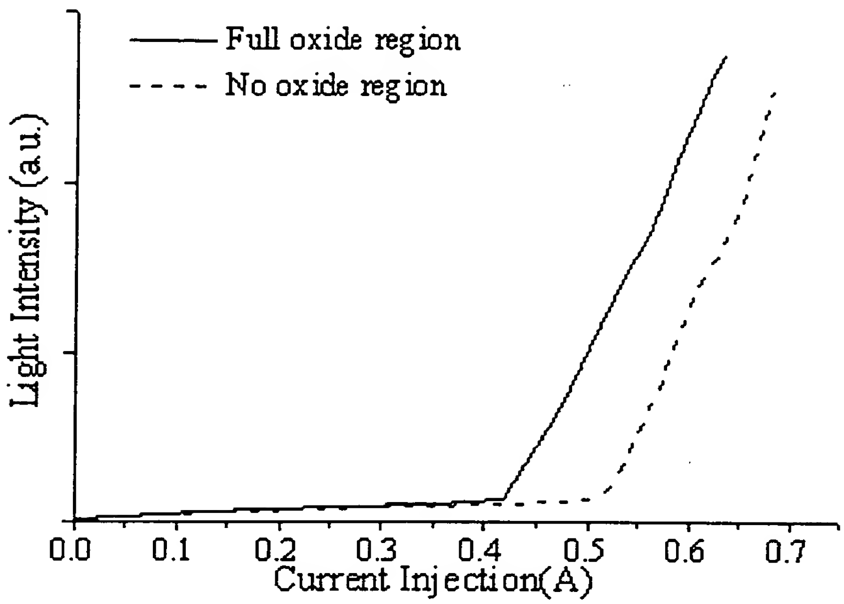


Figure 4(c)

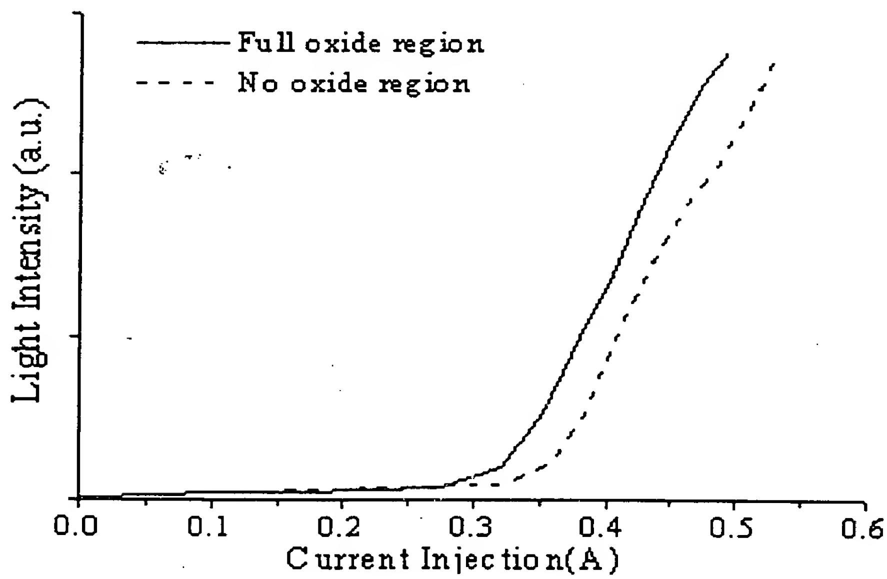


Figure 5(c)